LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-40 (canceled)

41. (previously presented) A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches;

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; and

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches;

wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE; and

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

42. (previously presented) A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches;

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; and

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches;

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches containing a gate structure and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

43. (previously presented) The device of claim 42, wherein said concentric ring-shaped trenches have a predetermined spacing from one another.

44. (previously presented) The device of claim 43, wherein the spacing between said concentric ring-shaped trenches is selected such that breakdown caused by high reverse voltage occurs between said concentric ring-shaped trenches before breakdown occurs in said active area.

45. (Previously presented) A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches; and

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; and

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches;

wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE; and

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches and said plurality of intermediate trenches defining an active area; said termination structure comprising at least a ring-shaped trench surrounding said active area and extending from said active area toward the edge of said die; said ring-shaped trench having a diffusion extending from its walls and bottom which is of said opposite conductivity type; said ring-shaped trench having a conductive polysilicon plug of said

opposite conductivity type; said ring-shaped trench being out of direct contact with said source contact and comprising a floating ring.

46. (previously presented) A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches; and

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches;

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches; and

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches and said plurality of intermediate trenches defining an active area; said termination structure comprising at least a ring-shaped trench

surrounding said active area and extending from said active area toward the edge of said die; said ring-shaped trench having a diffusion extending from its walls and bottom which is of said opposite conductivity type; said ring-shaped trench having a conductive polysilicon plug of said opposite conductivity type; said ring-shaped trench being out of direct contact with said source contact and comprising a floating ring.

47. (New) A MOS-gated semiconductor device comprising:

a semiconductor substrate of a first conductivity;

a drift region of said first conductivity formed over said substrate;

a channel region of second conductivity formed over said drift region;

a plurality of first trenches formed through at least said channel region;

gate insulation disposed on sidewalls of said plurality of first trenches;

a polysilicon gate electrode formed in each of said first trenches;

a second trench formed adjacent each said first trench, said second trench extending through said channel region and reaching at least said drift region;

a polysilicon body of said second conductivity formed in each said second trench;

a region of said second conductivity in said drift region adjacent each polysilicon body of said second conductivity;

conductive regions of said first conductivity formed adjacent each of said first trenches in said channel region; and

an electrode in electrical contact with said conductive regions and said polysilicon bodies of said second conductivity.

48. (New) A MOS-gated semiconductor device according to claim 47, wherein said gate insulation is comprised of silicon dioxide characterized by being resistant to radiation damage due to total radiation dose.

49. (New) A MOS-gated semiconductor device according to claim 48, wherein said gate insulation is less than 900Å.

50. (New) A MOS-gated semiconductor device according to claim 48, wherein said gate insulation is about 500Å.

51. (New) A MOS-gated semiconductor device according to claim 47, further comprising an insulation layer disposed at the bottom of each of said first trenches, said insulation at the bottom of each said first trench being thicker than said gate insulation on said sidewalls of said first trenches.

52. (New) A MOS-gated semiconductor device according to claim 51, wherein said insulation at the bottom of each of said first trenches is comprised of silicon dioxide characterized by being resistant to SEE.

53. (New) A MOS-gated semiconductor device according to claim 52, wherein said insulation at the bottom of each of said first trenches is thicker than 1300Å.

54. (New) A MOS-gated semiconductor device according to claim 52, wherein said insulation at the bottom of each of said first trenches is at least 3000Å thick.

55. (New) A MOS-gated semiconductor device according to claim 47, wherein said polysilicon gate electrodes are of said first conductivity.

56. (New) A MOS-gated semiconductor device according to claim 47, further comprising a termination structure formed around said plurality of first trenches.

57. (New) A MOS-gated semiconductor device according to claim 56, wherein said termination structure comprises a plurality of spaced trenches each forming a ring around said plurality of first trenches and each having a polysilicon body of said second conductivity disposed therein.

58. (New) A MOS-gated semiconductor device according claim 47, wherein said conductive regions of said first conductivity are source regions and said electrode is a source contact.